REMARKS

The following is intended as a full and complete response to the Office Action dated February 16, 2010, having a shortened statutory period for response set to expire on May 16, 2010. The Examiner objected to the abstract of the specification for failing to comply with MPEP §608.01(b). The Examiner rejected claims 1-11 and 13-28 under 35 U.S.C. §103(a) as being unpatentable over Van Hook (U.S. Patent No. 6,342,892) in view of Suzuoki ("A Microprocessor with a 128-bit CPU"). The Examiner also rejected 12 under 35 U.S.C. §103(a) as being unpatentable over Van Hook in view of Suzuoki and Intel (Intel PCI and PCI Express).

Objection to the Specification

The Examiner objected to the abstract of the specification for failing to comply with MPEP §608.01(b). Specifically, the Examiner states that the abstract, as originally filed, failed to accurately describe the technical details of the patent application. In this response, Applicants have amended the specification to include a new abstract that properly captures the inventive aspects of the patent application. Applicants, therefore, respectfully request the withdrawal of the objection to the abstract of the specification.

Rejections under 35 U.S.C. §103(a)

Amended claim 1 recites the limitations of a hardware-based physics processing unit (PPU) comprising a PPU control engine (PCE) configured to control the overall operation of the PPU by allocating memory resources within an internal memory to a floating point engine (FPE) and distributing commands received from a host central processing unit (CPU) to the FPE for processing. These amendments are supported by at least paragraphs [0064] and [0070] of the Application, as originally filed. None of the cited references teaches or suggests these limitations.

Van Hook discloses a coprocessor that includes a signal processor, a display processor and multiple interface units for communicating with components external to the coprocessor. One such interface unit is the CPU interface, which facilitates the transmission of data and memory addresses between the coprocessor and the CPU (see Van Hook at Figure 5 and Figure 38). The CPU interface includes a FIFO buffer that provides bidirectional buffering between the CPU and a data bus internal to the

coprocessor. The CPU interface also includes a control block that receives addresses from the CPU and pushes the address onto an address bus internal to the coprocessor. The control block also receives interrupt and control signals from the CPU as well as the signal processor and the display processor.

In the Office Action, the Examiner equates the disclosed coprocessor to the claimed PPU and the disclosed signal processor to the claimed FPE. The Examiner then generally points to the coprocessor architecture disclosed in Van Hook, without any specific explanation, as teaching the claimed PCE. Applicants contend, however, that there is no specific element within the Van Hook coprocessor that performs the function of the claimed PCE, as recited in amended claim 1. More specifically, none of the components within the coprocessor controls the overall operation of the coprocessor by allocating memory resources within an internal coprocessor memory to the signal processor. The interface units are simply communication gateways between external components and the coprocessor and do not perform any memory allocation operations. Similarly, Van Hook does not teach or suggest that the signal processor or the display processor perform any memory allocation operations. For this reason, Van Hook fails to teach or suggest the limitations of the PCE within the PPU configured to control the overall operation of the PPU by allocating memory resources within the internal memory to the FPE, as expressly recited in amended claim 1.

Both Suzuoki and Intel fail to cure the deficiencies of Van Hook set forth above.

As the foregoing illustrates, no combination of the cited references teaches or suggests each and every limitation of claim 1. Therefore, these references cannot render obvious claim 1 or claims 4-8, dependent thereon. For this reason, Applicants submit that claims 1 and 4-8 are in condition for allowance.

In addition, claim 9 is amended to recite limitations similar to those discussed above in conjunction with claim 1. Therefore, amended claim 9 is allowable for at least the same reasons as allowable claim 1. Further, claims 10-12 and 16-28 depend on claim 9 and are also in condition for allowance.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Office Action mailed February 16, 2010 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

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